Confirmation No. 4657

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	LEIJTEN	Examiner:	Giroux, G.
Serial No.:	10/511,512	Group Art Unit:	2183
Filed:	October 14, 2004	Docket No.:	NL020321US
Title:	REGISTER SYSTEMS AND METHODS FOR A MULTI-ISSUE PROCESSOR		

APPEAL BRIEF

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 26, 2008 and in response to the rejections of claims 1-7 as set forth in the Final Office Action dated July 28, 2008.

Please charge Deposit Account number 50-0996 (NXPS.305PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 016336/0856 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-7 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated July 28, 2008.

V. Summary of Claimed Subject Matter

Appellant's invention is related to a receiver that is designed for use with radio frequency signals situated in multiple frequency bands.

Commensurate with independent claim 1, a multi-issue processor comprises a register file (*see, e.g.*, FIG. 1, RF_0 or RF_1 and Appellant Specification (as originally filed) at page 4, line 30 to page 5 line 4) and a plurality of issue slots (*see, e.g.*, FIG. 1, UC_0-UC_3 and Appellant Specification at page 4, line 30 to page 5 line 6). Each one of the plurality of issue slots including a plurality of functional units (*see, e.g.*, FIGs. 2-3, FU_0-FU_2 and Appellant Specification at page 5, lines 5-28), an input routing network (*see, e.g.*, FIGs. 2-3, IRN and Appellant Specification at page 5, lines 5-28) that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to

functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths, and a plurality of holdable registers (*see, e.g.*, FIGs. 2-3, elements 1, 3, 5, 101, 103, and 105 and Appellant Specification at page 5, line 28 to page 6, line 28) that hold duplicate data from the register file, wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set (*see, e.g.*, FIG. 2, elements 1, 3, and 5 and Appellant Specification at page 5, line 28 to page 6, line 28) and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set (*see, e.g.*, FIG. 3, elements 101, 103, and 105 and Appellant Specification at page 5, line 28 to page 6, line 28).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1, 3 and 4 stand rejected under 35 U.S.C. § 103(a) over the Slavenburg reference (U.S. Patent No. 6,122,722) in view of the Martonosi reference (U.S. Patent No. 6,745,336).

B. Claims 2 and 5-7 stand rejected under 35 U.S.C. § 103(a) over the Slavenburg and Martonosi references in further view of the Fisher reference (U.S. Patent No. 6,026,479).

VII. Argument

1) Overview

As a precursor to the arguments presented below, Appellant notes that a key element of the instant Appeal and of Appellant's claimed invention relates to proper placement of holdable registers. The Examiner simply concludes that the prior art would be modified to conform to this key element. The Examiner provides neither evidence nor argument to support this conclusion. Moreover, the record is rife with evidence of why the skilled artisan would not seek to implement the proposed modification. In this light, the main issues for this Appeal are as follows:

- The combination of references fails to teach or suggest each element including aspects relating to the particular placement of the holdable registers.
- The proposed combination does not confer the benefits of power savings, which forms the basis for the alleged motivation.
- The references teach away from the proposed modification, which would frustrate the purpose of the primary reference.

A holding favorable to the Appellant for any one of these issues renders each of the rejections improper. Accordingly, Appellant will address each issue in turn. First, however, a brief overview of the teachings of Appellant's claimed invention and the asserted references is provided.

Aspects of the claimed invention relate to careful placement of holdable registers within a multi-issue processor. As discussed in Appellant's specification, multi-issue processors contain multiple functional units. Depending upon the current instruction, one or more of the functional units might not be used each cycle. Thus, one aspect of the invention uses a set of holdable registers located at the input of the functional units. Thus, when a functional unit is not used, the input remains constant, thereby reducing power consumption of the functional unit. Other aspects of the present invention recognize that when an interrupt event occurs, the presence of such holdable registers means that a large amount of data needs to be stored before the interrupt event can be processed. Thus, a second set of holdable registers is implemented before a routing network. The routing network provides multiple data outputs for a single data input and therefore, the total number of registers is less when

placed before the routing network. As discussed in Appellant's specification, the second set of holdable registers can be used in connection with an issue slot that is associated with interrupts.

The Examiner relies upon a modification of the very long instruction world (VLIW) processor of the Slavenburg reference. For convenience, FIG. 3 of the Slavenburg reference is reproduced below.

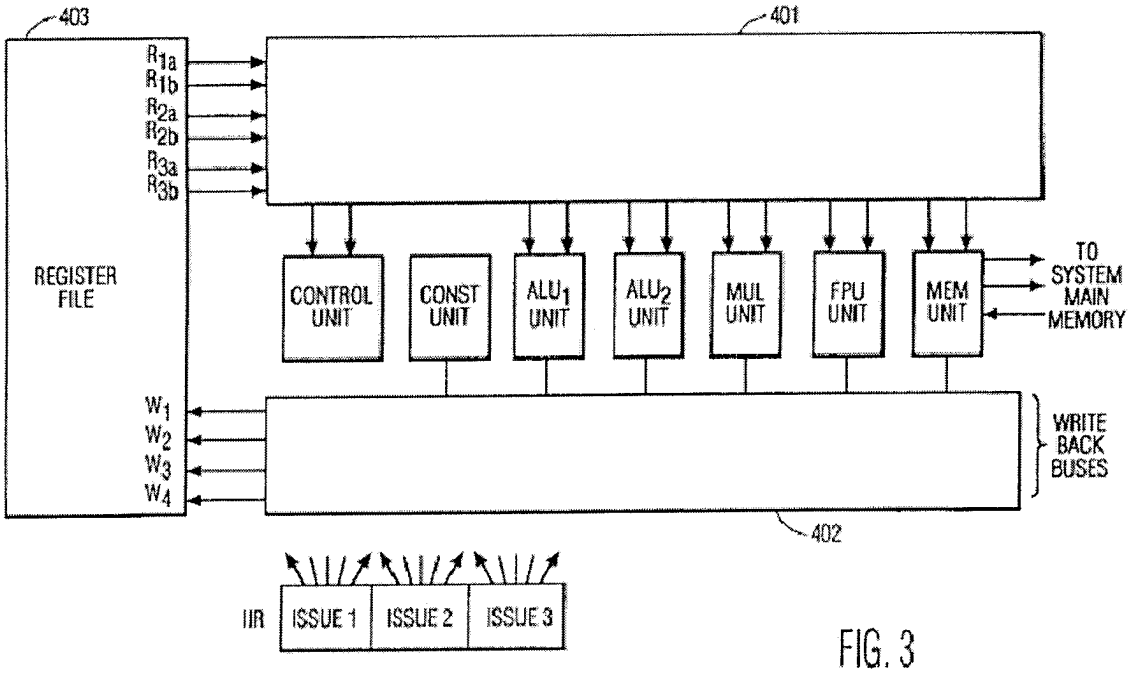

FIG. 3

Slavenburg teaches that issues 1-3 control the output of registers R1-R3 and the routing of the output to the various functional units using switching matrix 401 (*see, e.g.*, Slavenburg, FIG. 3).

Martonosi, as relied upon by the Examiner, teaches a set of latches that are used to disable a predetermined number of unused bits within a single operand. Martonosi teaches that when zero bits are detected in the uppermost bits of an operand, those bits can be disabled by maintaining the currently latched value (*see, e.g.*, Martonsi at Col. 5, lines 1-13). For convenience, FIG. 1 of the Martonosi reference is reproduced below.

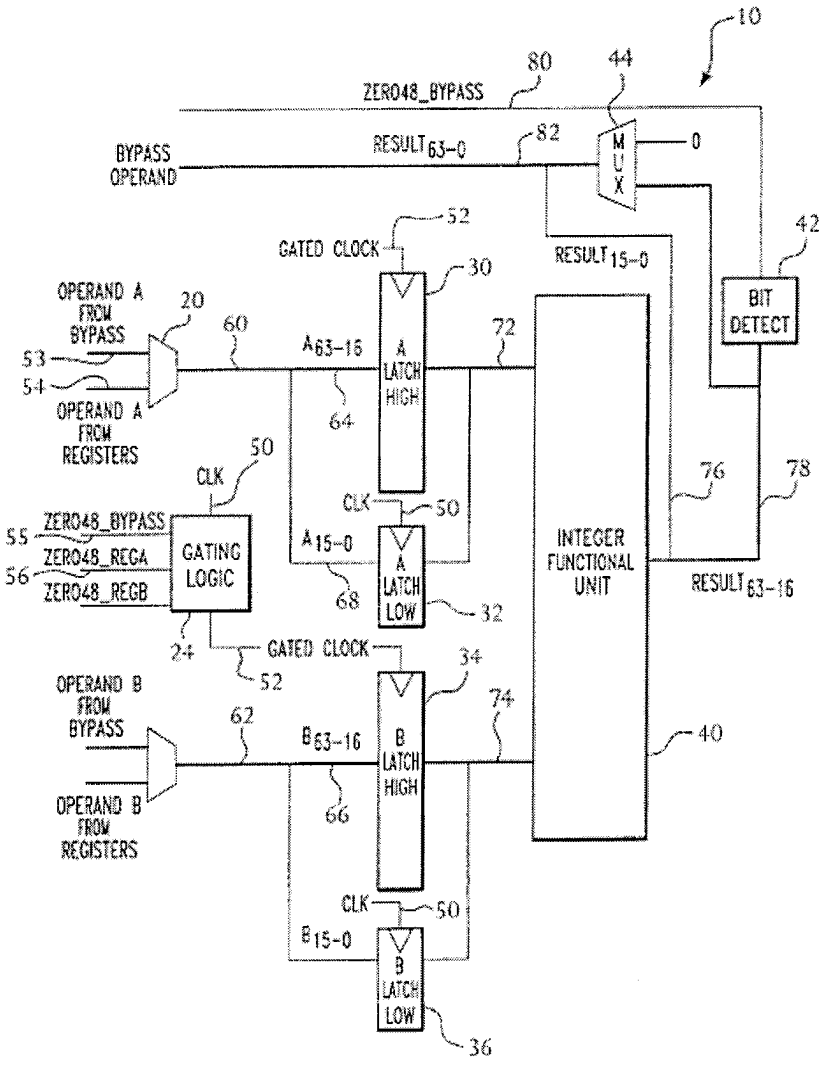

FIG. 1

Martonosi does not teach nor suggest applications for use with a VLIW processor and the associated circuitry, such as the routing matrix 401 and multiple functional units of Slavenburg. Instead, Martonosi teaches that the gating of latches 30, 34 is controlled by bit detectors that detect when portions of the operand are zeroes. The disclosure of Martonosi centers around addressing problems associated with variable-sized operands as is found in pipelined processor (*see, e.g.*, Martonosi at Col. 5, lines 64-65 ("'Intel x86', 'Motorola 68k', and 'IBM/Motorola Power PC'")).

2) The Rejections Of Claims 1, 3 And 4 Under 35 U.S.C. § 103(a) Over The Slavenburg Reference In View Of The Martonosi Reference Are Improper And Should Be Reversed.

The following subsections explain the impropriety of the rejections. Each of the subsections presents an independent and sufficient reason why the rejections are improper and should be reversed.

a) The Combination Of References Is Improper Because Correspondence To Each Claim Element Has Not Been Shown.

The Examiner has not shown that each claim element is present in the cited references. Rather than finding support for each claim element in the prior art, the Examiner effectively dismisses various claim limitations as "purely a matter of design choice." The Examiner does not provide evidence of any suggestion or motivation for the limitations, nor does the Examiner clearly articulate a reason for the proposed deviation from the teachings of the references. Accordingly, there is not sufficient evidence to establish a *prima facie* case of obviousness.

Obviousness cannot be established by merely alleging that a worker in the art could perform the proposed modification (*e.g.*, purely a matter of design choice). Design choices are not inherently obvious (many, if not all, inventions stem from a choice made in the design of the invention). It is well established that obviousness cannot be shown simply because a combination of elements is possible. "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984). The U.S. Supreme Court has recently explained that most, if not all, inventions are combinations of what was in some sense already known. The U.S. Supreme Court further clarified that an assertion of obviousness requires that there be a clearly articulated reason for the proposed modification. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (U.S. 2007). Summary conclusions about the obviousness of a modification (*e.g.*,

merely a design choice) do not meet these standards for obviousness. Using such a general standard, it is difficult to envision any circuit that would not be the result of a "design choice" of circuit elements and their placement. Thus, it is improper for the Examiner to conclude that the claimed invention is obvious because one or more modifications were "purely a design choice."

Moreover, these limitations are not an obvious variant of an unimportant element. The Examiner has, instead, failed to address a key element of Appellant's claimed invention. Appellant's specification teaches that a number of advantages can be achieved through bifurcation of the power-saving registers into two different sets. For example, Appellant's specification teaches a first set corresponds to functional units associated with interrupt routines. For this set, the registers are placed at the input of the input routing network (*see, e.g.*, Appellant's Disclosure, FIG. 2). For functional units of a second set, the register placement is between the input routing network and the functional unit (*see, e.g.*, Appellant's Disclosure, FIG. 3).

The cited references neither hint nor suggest the particular placement of registers proposed by the Examiner. The Examiner does not attempt to remedy this failure with an articulated reason for modifying the teachings of Slavenburg to correspond to related limitations. The Examiner, instead, summarily concludes that the proposed modifications are merely a design choice and are therefore obvious. Neither the Examiner nor the references, however, provide any indication as to why such a "design choice" would be obvious to implement by the skilled artisan. The Examiner has done little more than assert that the modifications would have been possible. Accordingly, a *prima facie* case of obviousness has not been presented, and the rejections should be reversed.

b) The Rejections Are Improper Because The Proposed Combination Does Not Confer The Benefits Related To The Alleged Motivation For The Combination.

The Examiner's rationale for combining the references relies upon an alleged benefit that is not obtained by the modification. An assertion of obviousness requires a clearly articulated reason for the proposed modification. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398

(U.S. 2007). It logically follows that when the reason/motivation for the proposed modification is to achieve an alleged benefit, the rejection cannot stand if the benefit is not achieved by the proposed modification.

The Examiner's proposed modification is predicated on the alleged benefit "to reduce the power used in the microprocessor by disabling a predetermined number of bits that are not require for the execution in the functional unit, using the operands within the input latches". Office Action dated July 28, 2008 at page 5. The proposed modification, however, does not reduce power by disabling predetermined bits and is therefore improper.

The asserted combination is primarily based upon aspects taken from FIG. 3 of Slavenburg. These aspects include register file 403 and routing matrix 401. The Examiner proposes modifying Slavenburg to add latches from Martonosi in a manner that places at least some of the latches between register file 403 and routing matrix 401. To the extent that Martonosi teaches use of power-saving latches, the latches are gated in response to determining that a set of bits is all zeros or ones (*see, e.g.*, Martonosi at col. 4, lines 54-60 and FIG. 1, bit detect 42). Neither the references nor the Examiner explains the relevance of such teachings to the Slavenburg reference. The skilled artisan would not attempt to solve a problem that is not present in the processor of the Slavenburg reference, and the record contains no evidence that Slavenburg suffers from the problem that is attempting to be solved by Martonosi (*e.g.*, unused bits due to varying sizes of the operands).

Moreover, the placement of registers suggested by the Examiner is illogical. The details of the routing matrix 401 are shown in FIG. 5 of Slavenburg. As shown, data from each register can be passed to any one of the functional units in response to multiplexor control signals (*i.e.*, $M_0C - M_6C$). The Examiner's proposed modification would latch the register data before this routing occurs; however, since the routing would still change consistent with the next instruction, the data received by the functional units would vary even with the proposed modification. Since the data received at the functional units would change even with the Examiner's proposed modification, the proposed modification would not provide any power savings. Moreover, adding additional circuitry would likely add to the power consumption of the circuit as well as introduce an additional timing delay. Thus, the

skilled artisan would not implement the proposed modification for the purpose of saving power.

For the aforementioned reasons, there remains no clearly articulated reason for why the skilled artisan would implement the proposed modification, and thus, the rejections should be reversed.

c) The Rejections Are Improper Because The References Teach Away From The Proposed Combination And Therefore There Is No Motivation For The Combination.

The skilled artisan would recognize that the proposed modification would create issues related to timing delays and data consistency. These issues would adversely affect the operation of the primary of the device and unduly affect the complexity of the design and operation of the primary device. As discussed supra, there is little or no benefit (power savings) obtained by the addition of latches in the proposed manner. Thus, the evidence of the record would have led the skilled artisan away from the proposed modification.

Slavenburg teaches that data from the functional units can be used for various purposes. One of these purposes includes a write-back operation for storing data in the register file (*see, e.g.*, Slavenburg at Col. 7, line 5 *et seq.*). Slavenburg teaches the skilled artisan that the different functional units have different latencies (*see, e.g.*, Slavenburg at Col. 7, table I). To account for these latencies, Slavenburg teaches the use of a rather complex series register file write control unit (RFWC). The RFWC is implemented using a routing matrix. The matrix has columns for each of the register ports and rows for various latencies of the functional units. A priority encoder (PREN) is used to produce write port enable signals.

The Martonosi reference is not directed to VLIW processors, such as the VLIW processor the Examiner wishes to modify. The Martonsi teachings, relating to a single functional unit, are silent regarding issues that may arise from parallel execution of VLIW processors and with an instruction register having fewer ports than the number of functional units. The proposed latching of data would raise a number of undesirable issues including, but not limited to, timing problems with the RFWC, delays in the execution time of the VLIW processor, increased circuit complexity (resulting in increased power consumption),

and data consistency issues. Thus, from the standpoint of the skilled artisan, there is ample evidence of reasons not to implement the proposed modifications, whereas the record contains no reason for the skilled artisan to implement the proposed modifications.

Moreover, Appellant's claim limitations require that there be two different sets of registers, each implemented in different locations. No reason is presented for the skilled artisan to bifurcate the placement of these registers. Thus, it is improper to assert that the skilled artisan would implement two different locations for the registers.

3) The Rejections Of Claims 2 And 5-7 Under 35 U.S.C. § 103(a) Over Slavenburg In View Of Martonosi And Further In View Of Fisher Are Improper And Should Be Reversed.

Each of claims 2 and 5-7 depend from claim 1 and necessarily contain each of the limitations thereof. The further modifications in view of Fisher do not cure the deficiencies of the 35 U.S.C. § 103(a) rejection of claim 1 discussed above under Section Heading 2. Accordingly, the rejections of claims 2 and 5-7 are improper and should be reversed in view of at least these aforementioned deficiencies.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-7 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/511,512)

1. A multi-issue processor comprising:

a register file; and

a plurality of issue slots, each one of the plurality of issue slots including

a plurality of functional units,

an input routing network that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths, and

a plurality of holdable registers that hold duplicate data from the register file,

wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set.

2. A multi-issue processor according to Claim 1, wherein

a first instruction set accesses at least the first set of issue slots; and

a second instruction set accesses the second set of issue slots.

3. A multi-issue processor according to Claim 1, wherein

the input routing network of each of the plurality of issue slot has a plurality of data path inputs; and

in the second set of issue slots holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file.

4. A multi-issue processor according to Claim 1, wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units.

5. A multi-issue processor according to Claim 1, wherein the first set of issue slots are accessed by a first set of instructions for a very-large-instruction-word (VLIW) processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine.

6. A multi-issue processor according to Claim 5, wherein the second set of instructions has less instructions than the first set of instructions.

7. A multi-issue processor according to Claim 1, wherein the first set of issue slots has more issue slots than the second set of issue slots.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.